

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L28	87	((first or second or upper or lower or top or bottom) near5 (chip or die) near5 (mount or mounting or mounted or stack or stacking or stacked)) with electrode with hole	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/11 22:09
L29	1640402	((first or second or upper or lower or top or bottom) near5 (chip or die) near5 (mount or mounting or mounted or stack or stacking or stacked)) with electrode with hole with (wire or wiring or wired)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/11 22:09
L30	32	((first or second or upper or lower or top or bottom) near5 (chip or die) near5 (mount or mounting or mounted or stack or stacking or stacked)) with electrode with hole with (wire or wiring or wired)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/11 22:11
L31	199	((first or second or upper or lower or top or bottom) near5 (chip or die)) with electrode with hole with (wire or wiring or wired)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/11 22:12
L32	10	((first or second or upper or lower or top or bottom) near5 (chip or die)) with electrode with hole with (wire or wiring or wired) with interposer	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/11 22:13
L33	54	((first or second or upper or lower or top or bottom) near5 (chip or die)) with electrode with hole with (wire or wiring or wired) with (insulating or dielectric or interposer)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/11 22:14
L34	54	((first or second or upper or lower or top or bottom) near5 (chip or die)) with electrode with hole with (wire or wiring or wired) with (insulating or dielectric or interposer or nonconductive or non-conductive)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/12/11 22:14

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DERWENT-WEEK: 200279

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TITLE: Stacked chip package

INVENTOR: KIM, D G; PARK, T S

PATENT-ASSIGNEE: SAMSUNG ELECTRONICS CO LTD[SMSU]

PRIORITY-DATA: 2000KR-0072322 (December 1, 2000)

PATENT-FAMILY:

PUB-NO	PUB-DATE	LANGUAGE
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KR 2002042958 A	June 8, 2002	N/A
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APPLICATION-DATA:

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KR2002042958A	N/A	2000KR-0072322
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INT-CL (IPC): H01L023/28

ABSTRACTED-PUB-NO: KR2002042958A

BASIC-ABSTRACT:

NOVELTY - A stacked chip package is provided to reduce a thickness of the stacked chip package by using a thickness of a substrate.

DETAILED DESCRIPTION - The first and the second chip mounting holes(35,45) are formed in a center portion of an upper portion of a substrate(31) such as a printed circuit board, a ceramic substrate, and a tape-wired substrate. The first mounting hole(35) is larger than the second mounting hole(45). A stepped portion(35a) is formed in an inside of the first and the second chip mounting holes(35,45). The first chop(32) is adhered to the stepped portion(35a)

through the first chip mounting hole(35) by using an adhesive(33).
The first
chip(32) is connected with a wiring pattern of the substrate(31) by a
bonding
wire(34). The second chip(42) is adhered to a lower side of the
first chip(32)
through the second chip mounting space(45) by using an adhesive(43).
The
second chip(42) is connected with a wiring pattern of the
substrate(31) by a
bonding wire(44).

CHOSEN-DRAWING: Dwg.1/10

TITLE-TERMS: STACK CHIP PACKAGE

DERWENT-CLASS: U11

EPI-CODES: U11-E02A1;

